REMARKS

After entry of this Amendment, claims 32-34 and 37-89 will be pending. Claims 32, 34, 42, 45, 48, 49, 55-57, 59, 60, 67, and 70-74 have been amended to clarify the scope of the invention; new claim 89 has been added; claims 35 and 36 have been cancelled.

Applicant thanks the Examiner for allowing claims 80-84, 87, and 88, and for indicating that claims 71-76 would be allowable if rewritten in independent form. Applicant has amended the claims accordingly. Support for the new claim and claim amendments may be found, for example, in the originally filed claims and in Figs. 4A-4D and 7A and related text. No new matter has been added.

Rejection of claims under 35 U.S.C. § 102

Claims 32-38, 41, 44-47, 65, 66, 77-79, 85, and 86 are rejected under 35 U.S.C. § 102(b) as being anticipated by N. Sugii, et al., "Role of $Si_{1-x}Ge_x$ Buffer Layer on Mobility Enhancement in a Strained-Si n-Channel Metal-Oxide-Semiconductor Field-Effect Transistor," *Appl. Phys. Lett.*, Vol. 75, No. 19, pp. 2948-2950 (1999) ("Sugii").

Sugii appears to describe electron mobilities of various strained Si-based metal-oxide-semiconductor field-effect transistors ("MOSFETs"). *See* Sugii, abstract. The Examiner states Sugii teaches all of the limitations of amended independent claim 32. However, none of the cited art teaches a first compressively strained layer having an average surface roughness of no more than approximately 2 nm, as recited in amended independent claim 32. Rather, Sugii discloses only MOSFETs including strained Si layers on SiGe buffer layers. *See*, Sugii, Figure 1. Since Si has a smaller lattice constant than SiGe, the strained Si layers of Sugii can only be tensilely strained, and cannot fulfill the requirements of amended claims 32.

Applicant submits that, for at least the above reason, amended independent claim 32 and claims dependent therefrom are patentable over the cited art.

Claims 42, 43, and 48 are rejected under 35 U.S.C. § 102(b) as being anticipated by Sugii. Claims 42 and 48 have been rewritten to depend on independent claim 32, and Applicant submits that claims 42 and 48 and claims dependent therefrom are patentable for at least the reasons that independent claim 32 is patentable.

Claims 67-69 are rejected under 35 U.S.C. § 102(b) as being anticipated by Sugii. However, Sugii does not teach or suggest the step of providing device isolation regions

comprising a dielectric material, as recited in amended independent claim 67. Sugii is utterly silent as to the formation of any sort of device isolation regions, other than the statement "MOSFETs were fabricated by wet chemical isolation." *See* Sugii, p. 2949, left column, line 11. Notably, Sugii's Fig. 1, relied upon by the Examiner, depicts no device isolation regions of any kind. Certainly Sugii does not teach or suggest the formation of device isolation regions comprising a dielectric material, as required by amended independent claim 67.

Applicant submits that, for at least the above reason, amended independent claim 67 and claims dependent therefrom are patentable over the cited art.

Rejection of claims under 35 U.S.C. § 103

Claims 38 and 40 are rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of Mizuno et al., "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," *IEEE Electron Device Letters*, Vol. 21, No. 5 (May 2000) ("Mizuno"). Mizuno appears to disclose methods of fabricating SiGe-on-insulator structures by the separation-by-implanted-oxygen ("SIMOX") technique. *See* Mizuno, abstract. Applicant submits that these claims are patentable at least for the reasons that independent claim 32, from which they depend, is patentable.

Claim 53 is rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of the Examiner's further remarks. Applicant submits that this claim is patentable at least for the reasons that independent claim 32, from which it depends, is patentable.

Claim 54 is rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of A. G. O'Neill, et al., "SiGe Virtual Substrate N-Channel Heterojunction MOSFETs," Semicond. Sci. Technol., Vol. 14, pp. 784-789 (1999) ("O'Neill 1999"). Applicant submits that this claim is patentable at least for the reasons that independent claim 32, from which it depends, is patentable.

Claim 39 is rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of Mizuno. The Examiner relies on Sugii to teach all of the limitations of independent claim 39, except for providing an insulating layer comprising SiO_2 disposed beneath a first strained layer. The Examiner relies on Mizuno to supply this feature, stating that it would have been obvious to one of ordinary skill in the art to modify the teachings of Sugii with those of Mizuno to form a FET structure with low parasitic capacitance, high carrier mobility, and simple isolation.

For the reasons that follow, we respectfully submit that the proposed combination would not be made by one of skill in the art, and, furthermore, that the function of Sugii's device is destroyed by the combination with Mizuno. Sugii specifically forms his strained Si-based structures on relaxed $Si_{1-x}Ge_x$, where x is 0.2 or 0.3, corresponding to 20% or 30% Ge. *See* Sugii, p. 2948, paragraph 3. Mizuno forms his structure by implanting oxygen ions into relaxed $Si_{0.9}Ge_{0.1}$ (i.e., 10% Ge) and annealing at 1350 °C. *See* Mizuno, p. 230, section II. Device Structure and Fabrication Processes, paragraph 1. The combination of the structure of Sugii with the method of Mizuno would result in the high temperature annealing of SiGe layers having 20% or 30% Ge at 1350 °C. However, this extreme temperature is higher than the melting point of SiGe alloys containing 20-30% Ge, as expressly shown by the solidus line of the Si-Ge phase diagram. *See* S. K. Ghandi, VLSI Fabrication Principles: Silicon and Gallium Arsenide, John Wiley & Sons, Inc.: New York, p. 74 (1994), attached hereto (*see* Appendix 1). The melting point of SiGe alloys containing 20-30% Ge falls between approximately 1200 °C and 1275 °C. Thus, it would not be obvious to one of ordinary skill in the art to apply the method of Mizuno to the structure of Sugii, as layers of Sugii's structure would melt and be rendered inoperative. Notably, Mizuno and his co-workers themselves admitted, in a subsequent publication, that their method is not usable with SiGe having a high Ge content. Mizuno et al. stated that "the melting point of SiGe layers with high Ge content is too low for the high temperature annealing of the SIMOX process," and that the Ge content of layers compatible with the process is limited to be lower than 14%. *See* p. 601, left column, paragraph 3 of T. Mizuno, et al., "Relaxed SiGe-on-Insulator Substrates without Thick SiGe Buffer Layers," Appl. Phys. Lett., Vol. 80, No. 4, pp. 601-603 (2002), attached hereto (*see* Appendix 2).

Thus, one of ordinary skill in the art would not combine the structures of Sugii with the methods of Mizuno. Therefore, we submit that, for at least these reasons, independent claim 39 and claims depending therefrom are patentable over the cited art.

Claim 43 is rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of the Examiner's further remarks. Applicant submits that this claim is patentable at least for the reasons that independent claim 32, from which it depends, is patentable.

Claims 49-52 and 59-64 are rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of O'Neill 1999. Claims 49, 59, and 60 have been rewritten to indirectly depend

on independent claim 32, and Applicant submits that claims 49, 59, and 60 and claims dependent therefrom are patentable for at least the reasons that independent claim 32 is patentable.

Claim 55 is rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of O'Neill 1999 and further in view of A. G. O'Neill, et al., "Deep Submicron CMOS Based on Silicon Germanium Technology," IEEE Trans. Electron Dev., Vol. 43, No. 6, pp. 911-913 (1996) ("O'Neill 1996"). Claim 55 has been rewritten to indirectly depend on independent claim 32, and Applicant submits that claim 55 is patentable for at least the reasons that independent claim 32 is patentable.

Claims 56-58 are rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of O'Neill 1996. Claims 56 and 57 have been rewritten to indirectly depend on independent claim 32, and Applicant submits that claims 56 and 57 and claims dependent therefrom are patentable for at least the reasons that independent claim 32 is patentable.

Claim 70 is rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of the Examiner's further remarks. Claim 70 has been rewritten to indirectly depend on independent claim 32, and Applicant submits that claim 70 is patentable for at least the reasons that independent claim 32 is patentable.

CONCLUSION

In light of the foregoing, Applicant respectfully submits that all claims are now in condition for allowance.

Applicant believes that no additional fees are necessitated by the present Response. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicant's agent would expedite allowance of this application, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,

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